

### **ADI Views on mmW 5G**



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- ►mmW 5G Goals
- Strategies to Achieve These Goals
- ▶ Beamforming
- mmW 5G Technical Challenges
- Architecture Discussion



### **Primary Goals for mmW 5G**

- Higher throughput
- ► Higher capacity
- ► Higher spectral efficiency
- ► Less latency
- ► Lower power

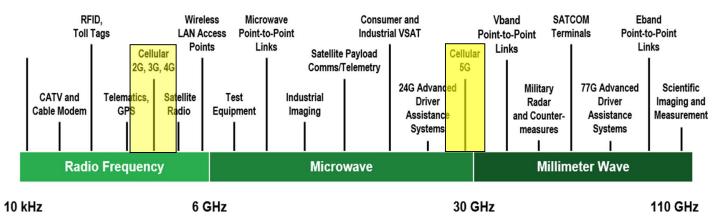




### How to Meet these Goals

- ► Build on 4G
  - OFDM-like Waveforms
  - Antenna Arrays
- ► Move to Higher Frequencies
  - Greater Bandwidth
    - More users; more throughput
  - Smaller Antennas
    - Allows higher antenna gains
  - Beamforming
    - Overcome higher path loss
    - Spatial isolation
    - Better use of spectrum
- Increase Integration

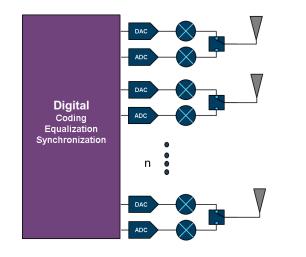






# **Beamforming Solutions**

Digital Beamforming (DBF)



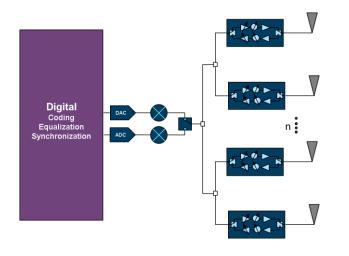
#### ► Pros

- Most flexible
- Most capacity
- Steer multiple beams and nulls

#### Cons

- Very high power and cost of digital processing / transport
- No spatial rejection from FE

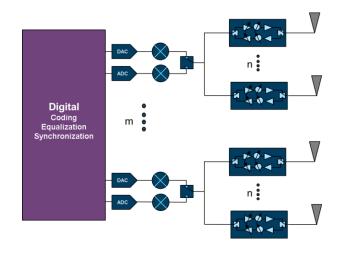
### Analog Beamforming (ABF)



► Pros

- Relatively low cost
- Much lower DSP
- Low power consumption
- Cons
  - Single beam
  - Single stream

#### Hybrid Beamforming (HBF)



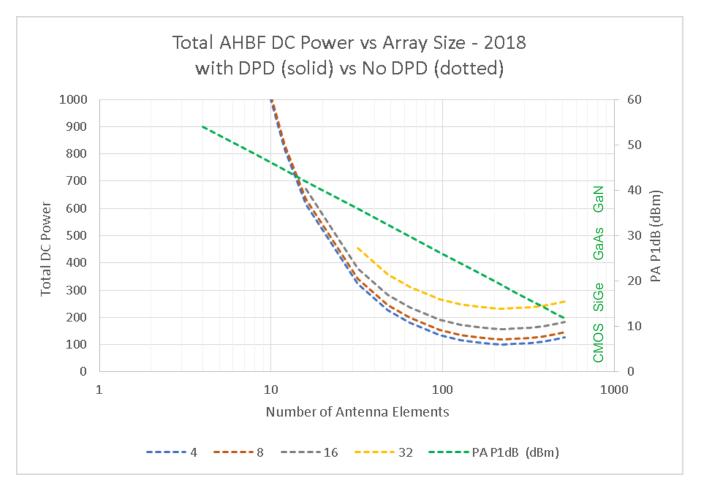
► Pros

- More capacity than ABF
- Much lower complexity / power than DBF
- Cons
  - Harder to perform MIMO processing



# Array Size Optimization for 60 dBm EIRP

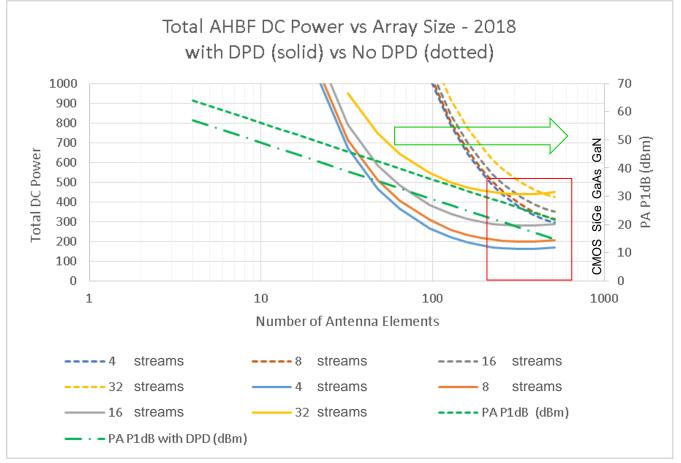
- Smaller arrays have less gain and therefore require more power per element
  - GaAs or GaN PAs dominate power consumption
  - DPD has large benefit
- Larger arrays have much higher gain and therefore require less power per element
  - Can be SiGe or CMOS (see green curves)
  - DPD has much smaller or even negative impact!
- Conclusion
  - With DPD: 64-128 elements
  - Without DPD: 128-256 elements
  - High power PA's not optimal!





### Array Size Optimization for 70 dBm EIRP

- Optimum array size
  - With DPD: about 256 elements with ≤22 dBm PAs
  - Without DPD: >512 elements with ≤20 dBm PAs





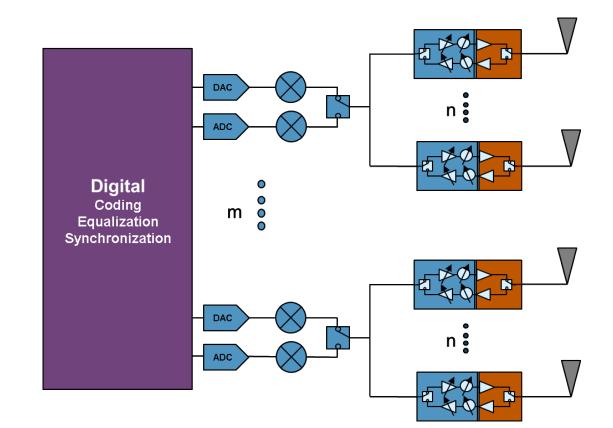
# Five Significant Challenges for mmW 5G

- Reduce digital power consumption to enable more capacity and move towards DBF
  - Data converters
  - JESD lanes
- Wideband DFE processing
  - QEC and CFR
  - Spur reduction/cancellation
- Improve PA efficiency
  - Currently ~2-4% for each antenna element without DPD
  - How to perform DPD over N PAs in sub-array
  - Or comparable PA efficiency technique (envelope tracking, Doherty, ...)
- Calibration of gain/phase to allow accurate beam steering and interference rejection
  - Within a sub-array
  - Between sub-arrays (to allow combining of sub-arrays)
  - Reduce or eliminate phase variation with gain (and gain variation with phase) to reduce calibration complexity
  - Phase synchronize multiple LO's over M streams
- Shrink mmW electronics to fit in back of antenna array
  - $\lambda/2$  between 4-6 mm for the 25 39 GHz bands



## **Chipset Architectures**

- ► HBF block diagram shown at right
- Macrocell may have individual chips for each function (including PA)
  - Many designs use a high IF configuration with digital board and microwave board
- CPE will support fewer (1?) stream and silicon PAs
- UE may have all functions integrated into one chip
- Can CPE chipset be used to construct Macro BTS?
- Will traditional PAs disappear from BTS designs?





# Summary

► Full DBF at mmW still a number of years off (if ever!)

- ADI actively investigating improved transceiver, converter and transport technologies
- ► HBF is currently most cost effective architecture to achieve mmW 5G goals
  - Different chipset architectures for the various use cases / applications
  - ADI has chipsets / technologies to form the complete HBF radio chain
- Looking to work with ecosystem partners and customers as the standards evolve toward high volume deployments





### **THANK YOU!**

ANALOG UEVICES

